

**REMARKS**

Applicant acknowledges with appreciation that the Examiner indicates that claims 9 and 10 would be allowable if rewritten in independent format, including the limitations of their base claim and any intervening claims. Applicant is amending the title of the invention. Claims 1-10 currently are pending and are subject to examination in the above-captioned patent application. Reconsideration of the above-captioned patent application is respectfully requested in view of the following remarks.

The Examiner objected to the title of the invention as allegedly being non-descriptive of the claimed invention. Applicant has amended the title of the invention, and respectfully submits that the amended title of the invention is descriptive of the claimed invention. Therefore, Applicants respectfully request that the Examiner withdraw the objection to the title of the invention.

The Examiner also rejected claims 1-8 under 35 U.S.C. § 102(b), as allegedly being anticipated by U.S. Patent No. 5,917,753 to Dallabora et al. ("Dallabora"). Applicant respectfully traverses these rejections, as follows.

Applicant's independent claim 1 describes a nonvolatile semiconductor memory device comprising "a reference load circuit which is **provided in each of said plurality of blocks**, and imposes a load on the reference signal that is identical to a load imposed on data that is read from said memory cell array." As such, in Applicant's claimed invention, a reference load circuit is provided in each block of the memory device.

Dallabora describes semiconductor memory device that uses a single reference column to supply a reference current to all of the sectors/blocks that share the single reference column. See, e.g., Dallabora, Column 2, Lines 27-32. The memory device also uses a double current mirror circuit (shown in Figure 3) to perform equalization independently for each sector/block without affecting the node of the single reference column. See, e.g., *Id.* at Column 4, Lines 60-68; and Column 5, Lines 1-29. Moreover, referring to Figures 2 and 3, the portion of memory device shown on the left-hand side of Figures 2 and 3 is shared by all of the sectors/blocks, while the portion of the memory device shown on the right-hand side of Figures 2 and 3 is provided within each of the sectors/blocks. In operation, a sense amplifier of each sector/block compares a data signal at a node B with a reference signal at a node A, thereby sensing data.

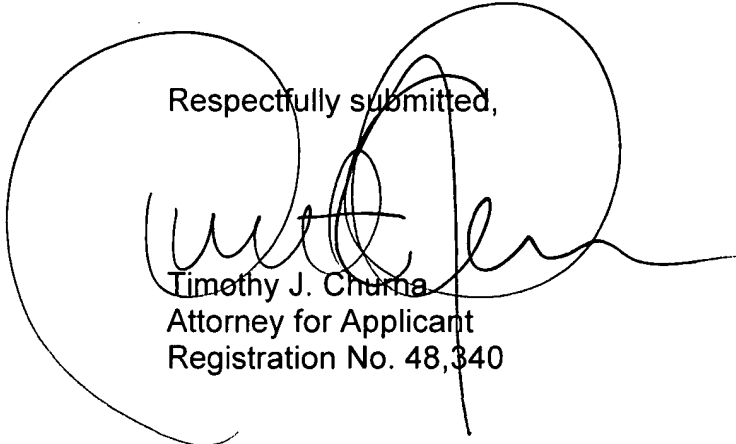
However, in Dallabora, the node A is connected to the sense amplifier of each sector/block so that the load (I/V Converter, Dummy Decoding) is **situated on the reference side**. Because the load is situated on the reference side and is not situated on the sector/block side, **the load is not provided in each of the sectors/blocks**, as set forth in Applicant's independent claim 1. Therefore, Applicant respectfully requests that the Examiner withdraw the anticipation rejection of independent claim 1 at least for this reason.

Claims 2-8 depend from allowable independent claim 1. Therefore, Applicant respectfully requests that the Examiner also withdraw the anticipation rejection of claims 2-8.

**CONCLUSION**

Applicant respectfully submits that the above-captioned patent application is in condition for allowance, and such action is earnestly solicited. If the Examiner believes that an in-person or telephonic interview with Applicant's representatives would expedite the prosecution of the above-captioned patent application, the Examiner is invited to contact the undersigned attorney of records. Applicant believes that no fees are due as a result of this submission. Nevertheless, in the event of any variance between the fees determined by Applicant and those determined by the U.S. Patent and Trademark Office, please charge any such variance to the undersigned's Deposit Account No. 01-2300.

Respectfully submitted,



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